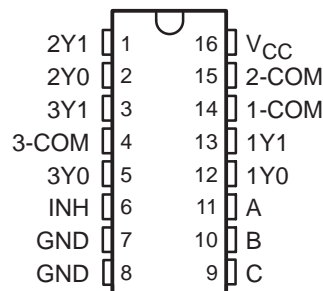


SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

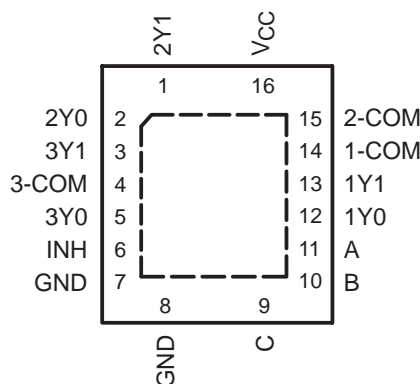
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- 2-V to 5.5-V V_{CC} Operation
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LV4053A . . . J OR W PACKAGE
SN74LV4053A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV4053A . . . RGY PACKAGE
(TOP VIEW)



description/ordering information

These triple 2-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV4053A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74LV4053AN	SN74LV4053AN
	QFN – RGY	Reel of 1000	SN74LV4053ARGYR	LW053A
	SOIC – D	Tube of 40	SN74LV4053AD	LV4053A
		Reel of 2500	SN74LV4053ADR	
	SOP – NS	Reel of 2000	SN74LV4053ANSR	74LV4053A
	SSOP – DB	Reel of 2000	SN74LV4053ADBR	LW053A
	TSSOP – PW	Tube of 90	SN74LV4053APW	LW053A
		Reel of 2000	SN74LV4053APWR	
Reel of 250		SN74LV4053APWT		
TVSOP – DGV	Reel of 2000	SN74LV4053ADGVR	LW053A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV4053AJ	SNJ54LV4053AJ
	CFP – W	Tube of 150	SNJ54LV4053AW	SNJ54LV4053AW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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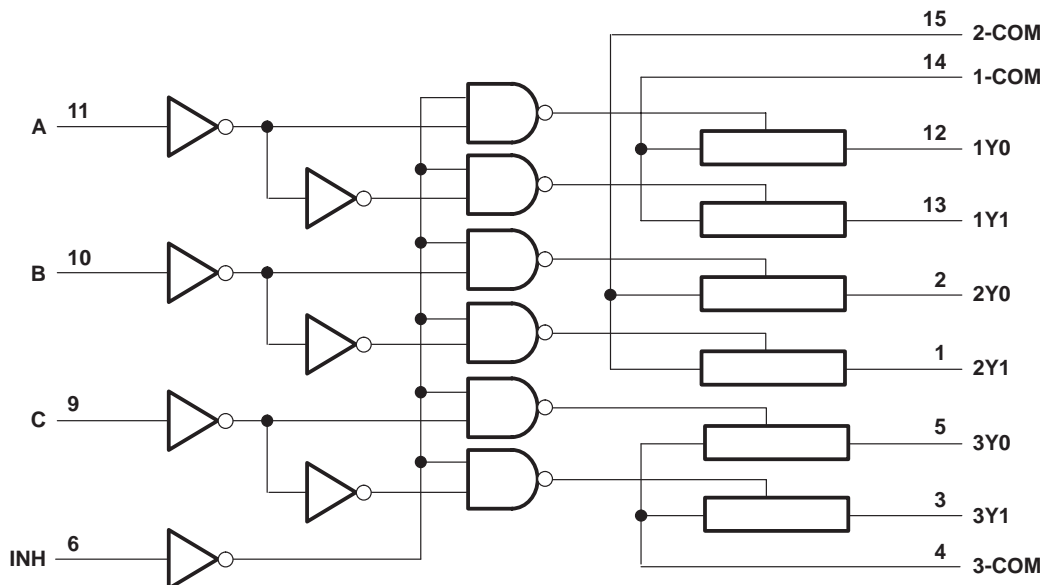
SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS430H – MAY 1999 – REVISED AUGUST 2003

FUNCTION TABLE

INPUTS				ON CHANNELS
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None

logic diagram (positive logic)



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SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS430H – MAY 1999 – REVISED AUGUST 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7.0 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)	± 50 mA
Switch through current, I_T ($V_{IO} = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

		SN74LV4053A		SN74LV4053A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2$ V	0.5	0.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
V_I	Control input voltage	0	5.5	0	5.5	V
V_{IO}	Input/output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	200	200		ns/V
		$V_{CC} = 3$ V to 3.6 V	100	100		
		$V_{CC} = 4.5$ V to 5.5 V	20	20		
T_A	Operating free-air temperature	-55	125	-40	85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS430H – MAY 1999 – REVISED AUGUST 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r _{on} On-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 1)	2.3 V	41	180		225		225	Ω	
		3 V	30	150		190		190		
		4.5 V	23	75		100		100		
r _{on(p)} Peak on-state resistance	I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V	139	500		600		600	Ω	
		3 V	63	180		225		225		
		4.5 V	35	100		125		125		
Δr _{on} Difference in on-state resistance between switches	I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V	2	30		40		40	Ω	
		3 V	1.6	20		30		30		
		4.5 V	1.3	15		20		20		
I _I Control input current	V _I = 5.5 V or GND	0 to 5.5 V			±0.1		±1	±1	μA	
I _{S(off)} Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 2)	5.5 V			±0.1		±1	±1	μA	
I _{S(on)} On-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IH} (see Figure 3)	5.5 V			±0.1		±1	±1	μA	
I _{CC} Supply current	V _I = V _{CC} or GND	5.5 V				20		20	μA	
C _{IC} Control input capacitance				2					pF	
C _{IS} Common terminal capacitance				8.2					pF	
C _{OS} Switch terminal capacitance				5.6					pF	
C _F Feedthrough capacitance				0.5					pF	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} Propagation delay time	COM or Y _n	Y _n or COM	C _L = 15 pF, (see Figure 4)	2.5	10		16		16	ns	
t _{PZH} Enable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	7.6	18		23		23	ns	
t _{PZL} Disable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	7.7	18		23		23	ns	
t _{PLH} Propagation delay time	COM or Y _n	Y _n or COM	C _L = 50 pF, (see Figure 4)	4.4	12		18		18	ns	
t _{PZH} Enable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	8.8	28		35		35	ns	
t _{PZL} Disable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	11.7	28		35		35	ns	

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SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULPLEXERS

SCLS430H – MAY 1999 – REVISED AUGUST 2003

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM	C _L = 15 pF, (see Figure 4)	1.6	6	10	10	10	ns	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	5.3	12	15	15	15	ns	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	6.1	12	15	15	15	ns	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM	C _L = 50 pF, (see Figure 4)	2.9	9	12	12	12	ns	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	6.1	20	25	25	25	ns	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	8.9	20	25	25	25	ns	

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM	C _L = 15 pF, (see Figure 4)	0.9	4	7	7	7	ns	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	3.8	8	10	10	10	ns	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	4.6	8	10	10	10	ns	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM	C _L = 50 pF, (see Figure 4)	1.8	6	8	8	8	ns	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	4.3	14	18	18	18	ns	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	6.3	14	18	18	18	ns	

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SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS430H – MAY 1999 – REVISED AUGUST 2003

analog switch characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	T _A = 25°C			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 6 and Figure 6)	2.3 V	30		MHz	
				3 V	35			
				4.5 V	50			
Crosstalk (between any switches)	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 7 and Figure 7)	2.3 V	-45		dB	
				3 V	-45			
				4.5 V	-45			
Crosstalk (control input to signal output)	INH	COM or Y _n	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 8)	2.3 V	20		mV	
				3 V	35			
				4.5 V	65			
Feedthrough attenuation (switch off)	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (see Note 7 and Figure 9)	2.3 V	-45		dB	
				3 V	-45			
				4.5 V	-45			
Sine-wave distortion	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 10)	V _I = 2 V _{p-p}	2.3 V	0.1		%
				V _I = 2.5 V _{p-p}	3 V	0.1		
				V _I = 4 V _{p-p}	4.5 V	0.1		

NOTES: 6. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads -3 dB.
7. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	5.3	pF

PARAMETER MEASUREMENT INFORMATION

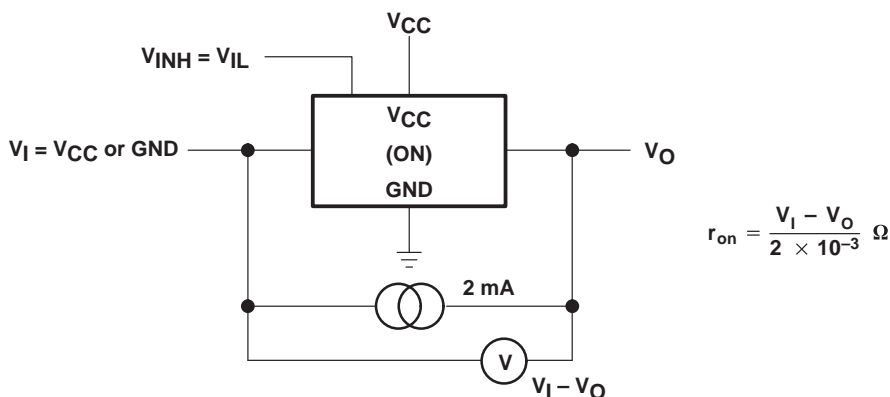


Figure 1. On-State Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION

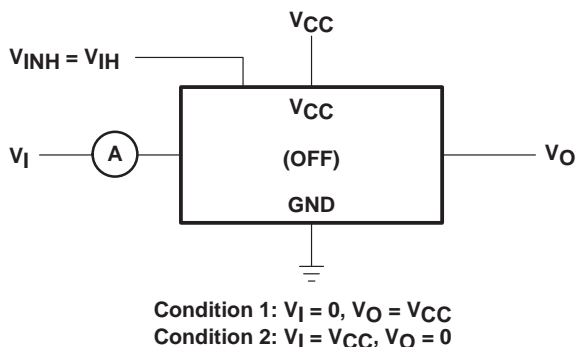


Figure 2. Off-State Switch Leakage-Current Test Circuit

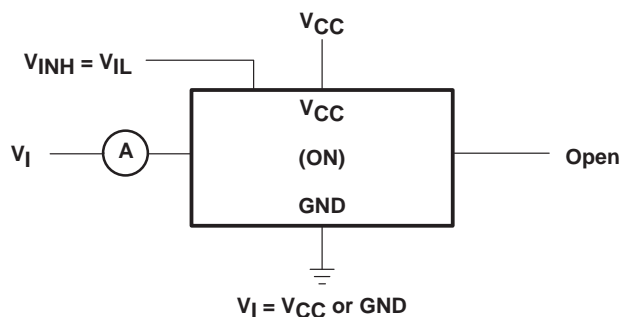


Figure 3. On-State Switch Leakage-Current Test Circuit

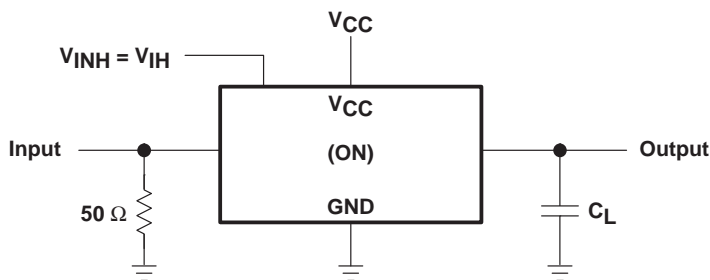


Figure 4. Propagation Delay Time, Signal Input to Signal Output

SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

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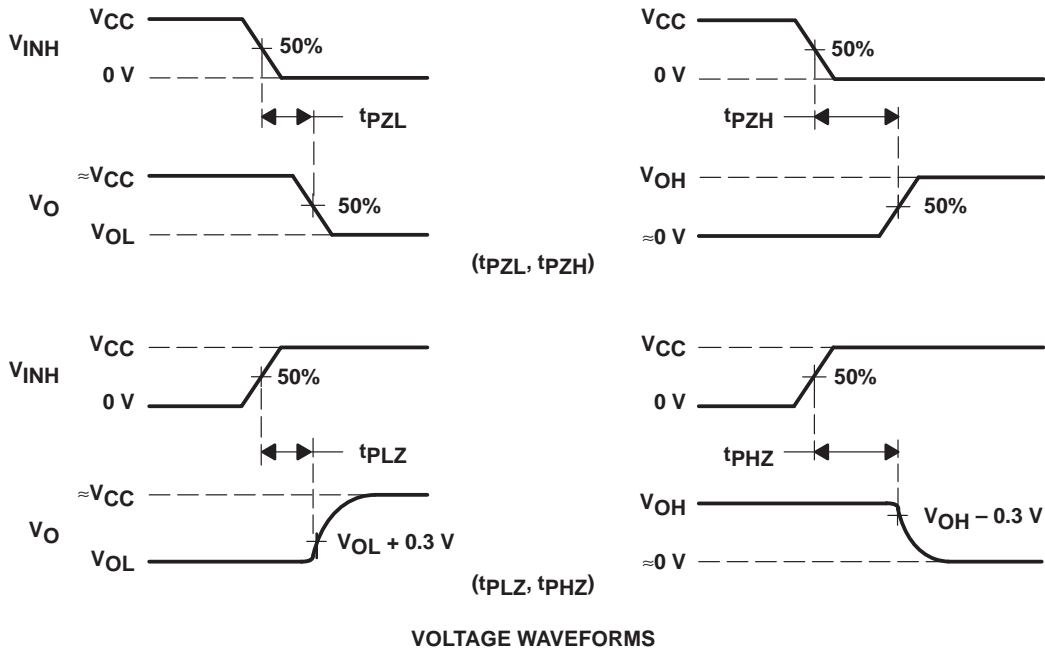
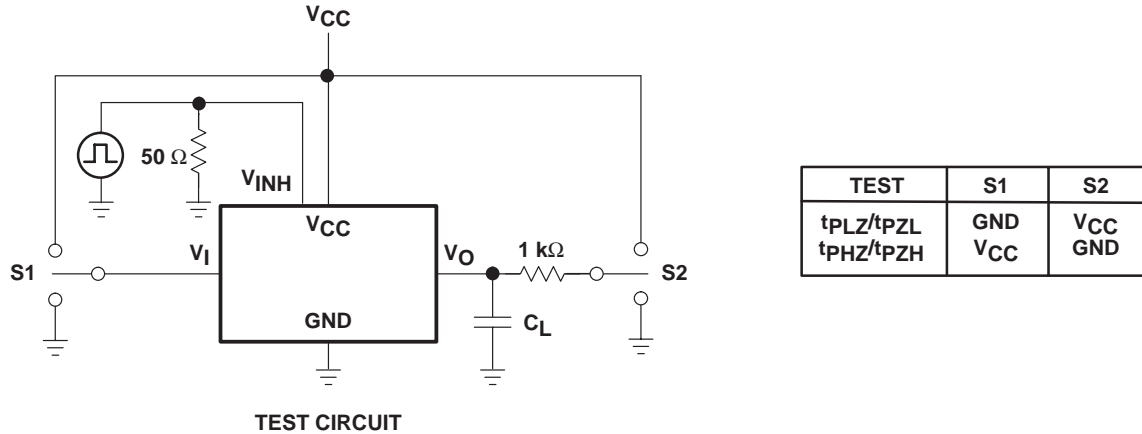
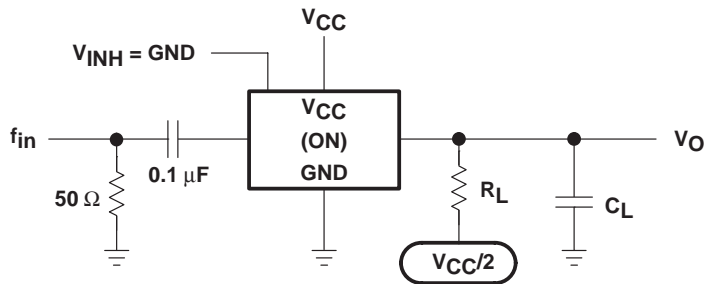


Figure 5. Switching Time (t_{PZL} , t_{PLZ} , t_{PHZ} , t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

PARAMETER MEASUREMENT INFORMATION

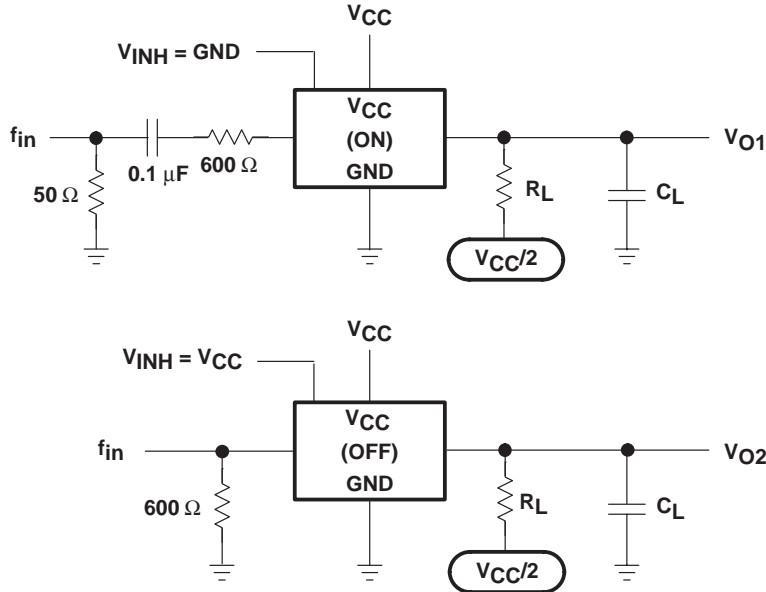


Figure 7. Crosstalk Between Any Two Switches

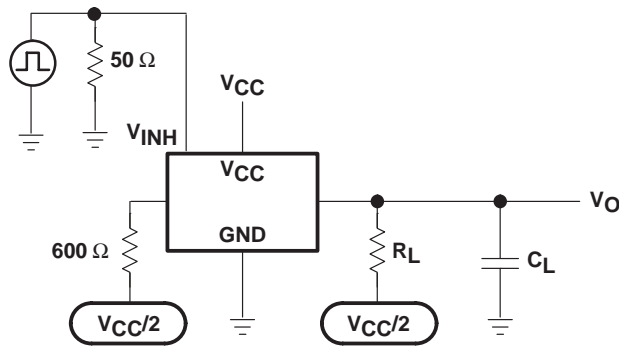


Figure 8. Crosstalk Between Control Input and Switch Output

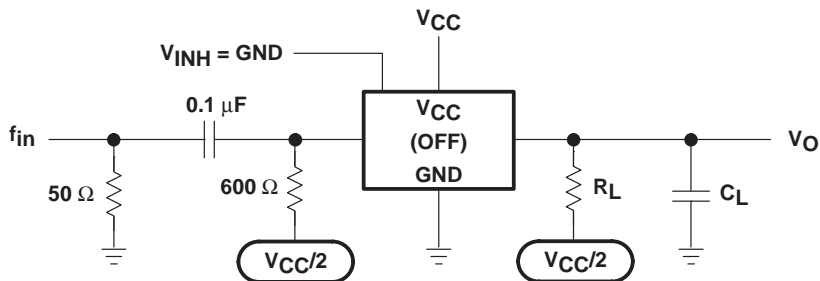


Figure 9. Feedthrough Attenuation (Switch Off)

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PARAMETER MEASUREMENT INFORMATION

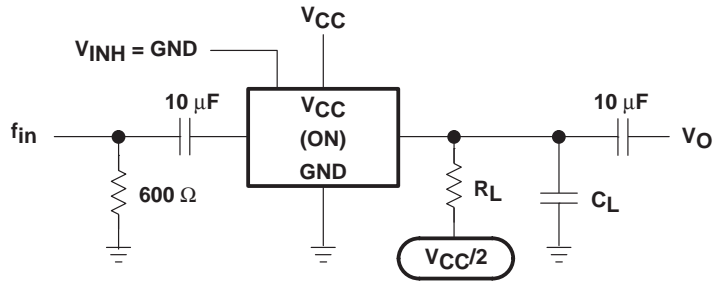
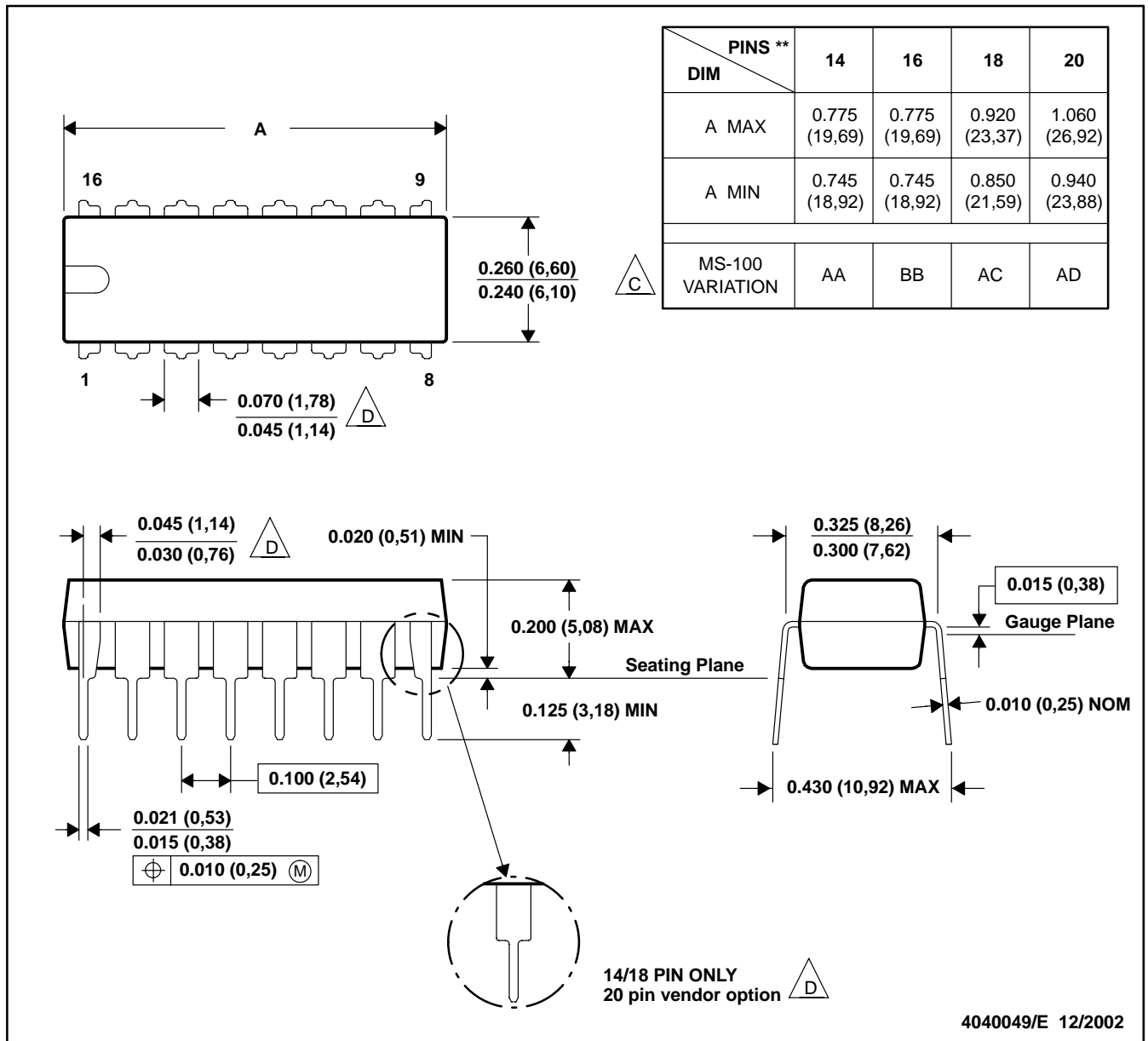


Figure 10. Sine-Wave Distortion

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

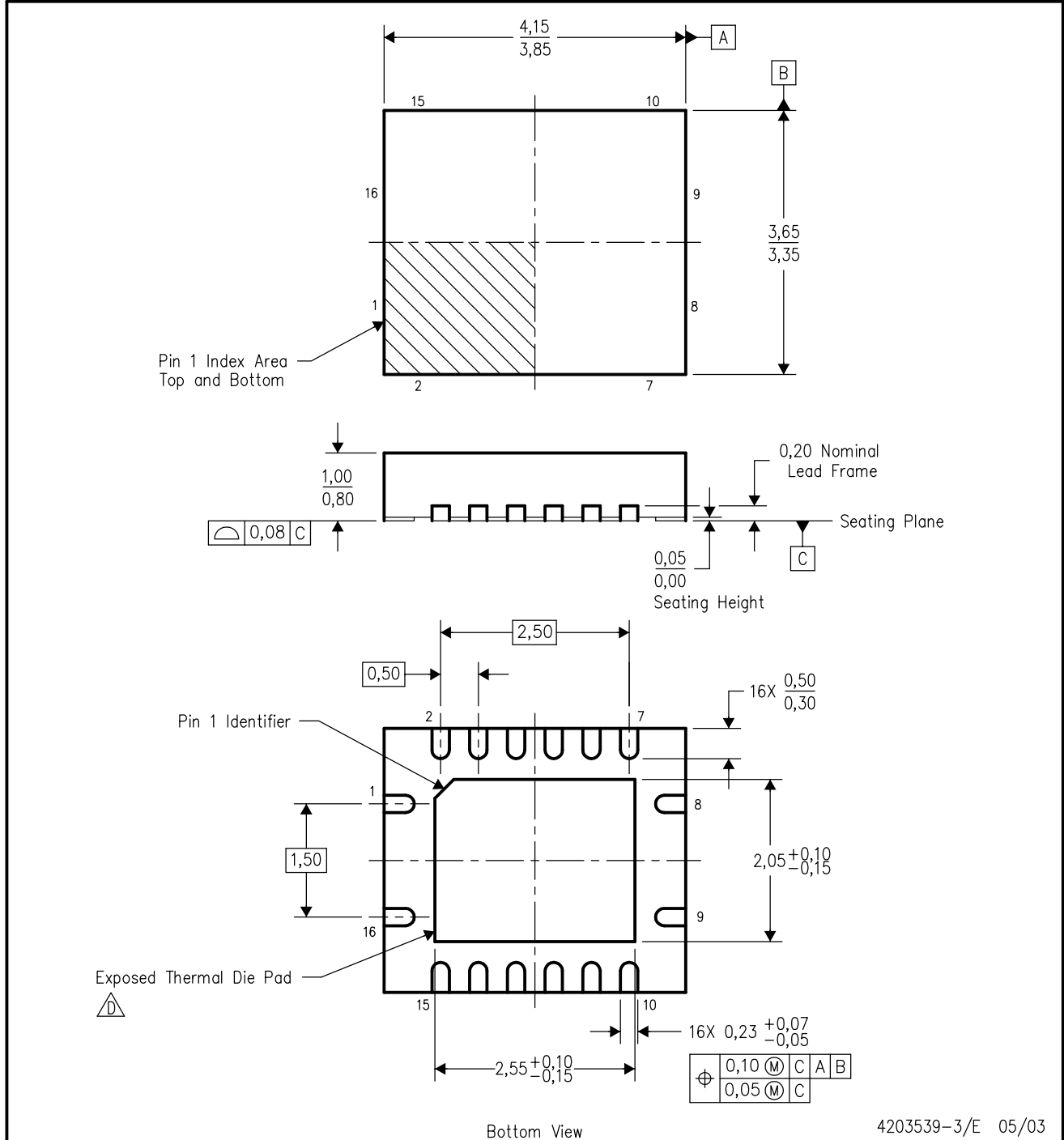
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194


RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



Bottom View

4203539-3/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BB.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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